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09/981,978	10/17/2001	Benjamin J. Parker	1567 (15721)	7499

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SPRINT COMMUNICATIONS COMPANY L.P.
6391 SPRINT PARKWAY
MAILSTOP: KSOPHT0101-Z2100
OVERLAND PARK, KS 66251-2100

EXAMINER	
SHEW, JOHN	
ART UNIT	**PAPER NUMBER**
2664	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,978	PARKER, BENJAMIN J.	
	Examiner	Art Unit	
	John L. Shew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/5/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-16* is/are allowed.

6)☒ Claim(s) *1,4,8 and 9* is/are rejected.

7)☒ Claim(s) *2,3,5-7 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al. (Patent No. 5008923) in view of Hatamian (Patent No. 6411117).

Claim 1, Kitamura teaches an apparatus comprising a first line interface for providing layer-1 interfacing to a communications trunk carrying a trunk signal (FIG. 9, col. 6 lines 59-67) referenced by the High-Speed Digital Line Interface Circuit 95 connecting to the High-Speed Digital Line at layer 1 the physical interface wherein the High-Speed Digital Line comprises multiplexed trunk circuits, a first framer coupled to said first line interface providing layer-2 interfacing to said trunk signal to make available frames of multiplexed individual subscriber signals (FIG. 9, col. 6 lines 59-67) referenced by the Multiplex Demultiplexer Unit 94 which connects to the High-Speed Digital Line Interface Circuit 95 to de-multiplex the trunk circuits 91n of individual subscribers, said individual subscriber signals each including respective transmit and receive signals (FIG. 9, FIG. 1, col. 2

lines 65-67, col. 3 lines 1-21) referenced by the transmit e(n) Out terminal 1d connection and the receive r(n) Input terminal 1a connection of the Testable Echo Canceller for connection to the Trunk Circuit 91n, and a test controller coupled to said first framer for continuously de-multiplexing said frames (FIG. 9, col. 6 lines 59-67) referenced by the Control Unit 93 coupled to the Demultiplexer Unit 94 via the respective Echo Cancellers 92n which is continuously connected to the de-multiplexed trunk lines of the High-Speed Digital Line.

Kitamura does not teach storing samples in a queue for a selected echo delay.

Hatamian teaches storing samples in a queue (Fig. 2, col. 4 lines 36-61, col. 7 lines 11-24) referenced by the LPBK FIFO 234 holding samples for the ECHO/NEXT Canceller 232, for a selected echo delay (FIG. 3A, col. 7 lines 61-67, col. 8 lines 1-13) referenced by the delay elements D_i of the Echo/NEXT Canceller implemented by a CMOS dynamic register, adding said samples to an individual receive signal for said selected individual subscriber signal after said selected echo delay (Fig. 2, col. 5 lines 45-67, col. 6 lines 1-12) referenced by the P/S MUX 224 from the Sampling Clock Domain which is sent to the Feed Forward Equalizer 26 where it is summed 32 with the output of the Echo/NEXT Canceller, and continuously re-multiplexing said frames (Fig. 2, col. 7 lines 11-48) referenced by the Gain Stage 34 output to the Deskew 36 and subsequent output to the Receive PCS 204R for transmission out.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dynamic register testing capability of Hatamian to the testable echo canceling method of Kitamura for the purpose of controlling voltages at

nodes that may become floating nodes in a dynamic register included in an integrated circuit as suggested by Hatamian (col. 2 lines 39-42).

Claim 4, Kitamura teaches a testable echo cancelling device with a test Controller (FIG. 1) referenced by the Control unit 15. Kitamura does not teach a test controller with selectable gain.

Hatamian teaches a controller comprising a selectable gain for adjusting a gain of said samples prior to adding them to an individual receive signal (Fig. 2, col. 4 lines 46-53) referenced by the Auto-Gain Control 220 adjusting the gain of the Line Interface prior to the summer 32 fo the Feed Forward Equalizer 26.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dynamic register testing capability of Hatamian to the testable echo canceling method of Kitamura for the purpose of controlling voltages at nodes that may become floating nodes in a dynamic register included in an integrated circuit as suggested by Hatamian (col. 2 lines 39-42).

Claim 8, Kitamura teaches a method for testing echo cancellers for connecting to individual terminals said individual terminals exchanging transmit and receive signals within a telecommunications system including a communications trunk (col. 2 lines 6-11, FIG. 1, col. 2 lines 65-67, col. 3 lines 1-21, FIG. 9, col. 6 lines 59-67) referenced by the Echo Cancellers 92_1 through 92n connecting to each individual terminal trunk with echo cancellation test circuitry connecting to transmit e(n) Out terminal 1d and receive r(n)

Input terminal 1a, said method comprising the steps of receiving respective transmit signals in said telecommunications system from each of said individual terminals (FIG. 9, col. 6 lines 59-67) referenced by the individual de-multiplexed trunk signals at the output of the Multiplex Demultiplexer Unit 94 from the High-Speed Digital Line of the telecommunications system, multiplexing a plurality of transmit signals into respective slots in a multiplexed signal (FIG. 9, col. 6 lines 59-67) referenced by the High-Speed Digital Line which is a multiplex of trunk line as reflected in the de-multiplexed trunk circuits 91n, coupling said multiplexed signal to a termination of said communications trunk (FIG. 9, col. 6 lines 59-67) referenced by the Trunk Circuits 91_1 through 91n which terminates the respective trunk of the multiplexed High-Speed Digital Line, connecting a test apparatus to said communications trunk (FIG. 9, Fig. 1, col. 2 lines 65-67, col. 3 lines 1-5) referenced by the Multiplexing Device 90 which contains for each Echo Canceller 92n a Call Signal Generation unit 12 in conjunction with the Test Echo Signal Generation unit 13, de-multiplexing said plurality of transmit and receive signals within said test apparatus (FIG. 1, FIG. 9) referenced by the Multiplex Demultiplexer Unit 94 which demultiplexes the trunk signals into a pair of transmit/receive signals for each Echo Canceller 92n, passing said receive signals through respective echo cancellers to generate echo-cancelled signals (FIG. 1, col. 2 lines 63-67, col. 3 lines 1-34) referenced by the Echo Sig s(n) terminal 1c passing through the Echo Canceller (DSP) unit 11 for output to e(n) Out terminal 1d to achieve echo cancellation, evaluating cancellation of said delayed echo signal by a corresponding echo canceller (FIG. 1, FIG. 4, col. 4 lines 3-16) referenced by the Residual Echo Detection unit 14 evaluating the echo power to a

determined threshold. Kitamura does not teach sampling a selected de-multiplexed transmit signal from its respective slot.

Hatamian teaches sampling at least one selected de-multiplexed transmit signal from its respective slot (Fig. 2, col. 4 lines 36-61, col. 7 lines 11-24) referenced by the LPBK FIFO 234 holding samples for the ECHO/NEXT Canceller 232, re-multiplexing said de-multiplexed transmit signals into said respective slots in a re-multiplexed transmit signal and coupling said re-multiplexed transmit signal to said communications trunk (Fig. 2, col. 5 lines 45-67, col. 6 lines 1-12, col. 7 lines 11-48) referenced by the P/S MUX 224 from the Sampling Clock Domain which is sent to the Feed Forward Equalizer 26 where it is summed 32 with the output of the Echo/NEXT Canceller followed by the , Gain Stage 34 output to the Deskew 36 and subsequent output to the Receive PCS 204R for multiplex transmission out, delaying said sampled signal by a selected echo delay to generate a delayed echo signal (FIG. 3A, col. 7 lines 61-67, col. 8 lines 1-13) referenced by the delay elements D_i of the Echo/NEXT Canceller implemented by a CMOS dynamic register, adding said delayed echo signal to a selected de-multiplexed receive signal corresponding to said selected de-multiplexed transmit signal (FIG. 2, FIG. 3A) referenced by the LPBK FIFO 234 which is the de-multiplexed signal to which the Echo Canc. 232 implements a series of delay elements, adding said delayed echo signal to a selected de-multiplexed receive signal corresponding to said selected de-multiplexed transmit signal (FIG. 2, col. 4 lines 37-61, col. 5 lines 45-65) referenced by the Receive PCS 204R corresponding to the Transmit PCS 204T which provides an input to the P/S MUX 224 for receiving the Echo Canceller 232 delayed signal through

the Summer 32, re-multiplexing said de-multiplexed receive signal in said test apparatus after said addition step and coupling said re-multiplexed received signal to said communications trunk ((Fig. 2, col. 7 lines 11-48) referenced by the Echo Canceller 232 delay signal to the Summer 34 followed by the Gain Stage 34 output to the Deskew 36 and subsequent output to the Receive PCS 204R for re-multiplexing transmission out, de-multiplexing said receive signal from said termination of said communications trunk to recover said receive signals (FIG. 2, col. 4 lines 36-52) referenced by the P/S Mux unit 224 de-multiplexing of receive signals from the termination of Line Interface 210 communication trunk to obtain receive signals.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dynamic register testing capability of Hatamian to the testable echo canceling method of Kitamura for the purpose of controlling voltages at nodes that may become floating nodes in a dynamic register included in an integrated circuit as suggested by Hatamian (col. 2 lines 39-42).

Claim 9, Kitamura teaches a testable echo cancelling device. Kitamura does not teach delaying a de-multiplexed transmit signal prior to re-multiplexing in response to a selected line delay.

Hatamian teaches the step of delaying a de-multiplexed transmit signal prior to re-multiplexing in response to a selected line delay (FIG. 2, FIG. 3A, col. 8 lines 65-67, col. 9 lines 1-4) referenced by the Echo Canceller 232 adding delay to the de-multiplexed Transmit signal via the LPBK FIFO 234 prior to re-multiplexing through the Summer 32

to the Receive PCS 204R wherein the Echo Canceller delay is based on the dynamic register.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dynamic register testing capability of Hatamian to the testable echo canceling method of Kitamura for the purpose of controlling voltages at nodes that may become floating nodes in a dynamic register included in an integrated circuit as suggested by Hatamian (col. 2 lines 39-42).

Allowable Subject Matter

2. Claims 11-16 are allowed.

Claims 2, 3, 5, 6, 7, 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

The arguments traversing the rejections of claims 1, 8 has been fully considered. The examiner respectfully disagrees. Kitamura teaches a first line interface, a first framer and a test controller as shown in Fig. 9 High-Speed Digital Line Interface Circuit 95, Multiplex Demultiplexer Unit 94 and Control Unit 93 respectively. There is no claim limitation pertaining to access to echo cancellers from a point where the subscriber signals are multiplexed together.

The Control Unit 93 does not interface directly to High-Speed Digital Line Interface Circuit 95, however this is not a cited limitation. The Control Unit 93 does couple to the Multiplex Demultiplex Unit 94 outputs to control the respective trunks through the Echo Cancellers which is consistent with the cited claim limitation.

Kitamura teaches in Fig. 1 a test echo signal generation device 13 within the Fig. 9 Echo Canceller 92n. The function of the Test Echo Signal Generation Device 13 is implemented as a separate unit within the Echo Canceller and as such is obvious it can be removed to be external to the unit. It is also obvious the function of the Test Echo Signal Generation Device 13 can be implemented within the Multiplex Demultiplex Unit 94 since the point at which the Test Echo Signal Generation Device 13 connects is between the output of the Multiplex Demultiplex Unit 94 and the input of the Echo Canceller 92n. The Control Unit 93 must be incorporated with the Test Echo Signal Generation Device as to provide the required control signals and as such would be part of the Test Echo Signal Generation Device if separated from the main Echo Canceller

unit. Separation of the units would then require external connection to the line signals for insertion of the Test Echo Signal.

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L. Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

js

Ajit Patel
Primary Examiner